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A DIGITAL DETECTOR WITH SELECTABLE PASSBAND.(U)
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TECHNICAL REPORT RC- 77-2

A DIGITAL DETECTOR WITH SELECTABLE PASSBAND

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3 January 1977

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Digital filters and detection techniques are used in many modern communication and control circuits. Such digital techniques are valued for ease of realization and implementation as well as for clean and precise logical outputs.

A digital detector can be designed with standard logic family components capable of detecting the center frequency, F_C, and bandpass, B, using standard Karnaugh mapping techniques.

An internal oscillaror at frequency F_o, provides a counting sequence C, to over

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ABSTRACT (Continued)

an "n-Bit" counter which provides the basis for nonsymmetrical "near ideal" filter. The basis of the filter is implemented on an "n-variable" Karnaugh map with the center frequency selected as the middle cell in an odd cellular array and the bandpass selected as the width of this cellular combination. Because standard Karnaugh mapping is used, the design process and logic relation is simplified by using a two level logic.

CONTENTS

SYMBOLS

B - Bandpass

C - The total count in the counter

Ca - The number of counts used in the Karnaugh map representation

C_k - The cell on the Karnaugh map that represents the center frequency of the incoming signal F_i.

e - Duty cycle of the pulses as detected by the counter

eTo - Proportional period depending on when the gating signal falls ($e > 0.5$)

F_C - The detected center frequency point of the incoming signal F_i

F_H - The detected high frequency cutoff point of the input signal F_i

F_i - Input signal frequency

F_{iH} - High end of passband

F_{iL} - Low end of passband

F_L - The detected low frequency cutoff point of the input signal F_i

F_o - Internal Oscillator Frequency

F' - Shift in the center frequency so as to make $+\Delta F' = -\Delta F'$

H - Harmonic (A positive integer number)

K - Total number of Karnaugh cells required to map the filter

K' - The number of Karnaugh cells as a function of C, P, and Q.

n - Number of full period counts as detected by counter

ne - A partial period of the count but is equal to a full count if $e > 0.5$

P - The number of Karnaugh cells above the center cell C

Q - The number of Karnaugh cells below the center cell C

T_i - Input frequency period

T_o - Internal gated pulse generator frequency period

T_x - Schmitt trigger "on" delay time

T_y - Schmitt trigger "off" delay time

T_z - Oscillator start delay time

Y - A multiple of C

2^a - Number of variables required to realize the Karnaugh mapping

$+\Delta F$ - Incremental increase in frequency above the center frequency

$-\Delta F$ - Incremental decrease in frequency below the center frequency

$+\Delta F'$ - Incremental increase in frequency above the center frequency to make $+\Delta F' = -\Delta F'$

$-\Delta F'$ - Incremental increase in frequency below the center frequency to make $-\Delta F' = +\Delta F'$

ω - Angular frequency

ω_c - Angular cutoff frequency

I. INTRODUCTION

Many kinds of filters exist, as do numerous ways of realizing these filters. Filters can be classified as passive, active, or digital. The passive filter realization is usually considered the classical type and may be defined as a selective network of resistors, inductors, or capacitors, offering comparatively little opposition to certain frequencies or to direct current, while rejecting or attenuating other frequencies. Additionally, a passive filter requires no external power supply. In recent years, with the advances in digital electronics and the operational amplifier, digital and active filters have been offering competition to the classical passive filters. The digital and active filters require a power supply. The active filters are used for analog signals, whereas the digital filters are used for digitized continuous signals. Various filter circuits and techniques have been developed to accomplish the task of selective frequency filtering that would approach the characteristics of the ideal filter as shown in Figure 1.

Figure 1, (a, b, and c) represents the ideal characteristics of a lowpass, highpass, and bandpass filter respectively.[1] The ideal lowpass filter amplitude characteristics are basically bounded by two straight right angle lines. The horizontal line of the filter characteristic represents the zero dB (Gain = 1) line from dc to the cutoff frequency, f_{oH}, and the vertical line represents the cutoff or stopband point for the amplitude of frequencies $f > f_o$. A similar description can be composed for the bandpass and highpass filter.

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[1] J. Millman and C. C. Halkias, Integrated Electronics: Analog and Digital Circuits and Systems (New York: McGraw-Hill Book Company, 1972) p. 548.

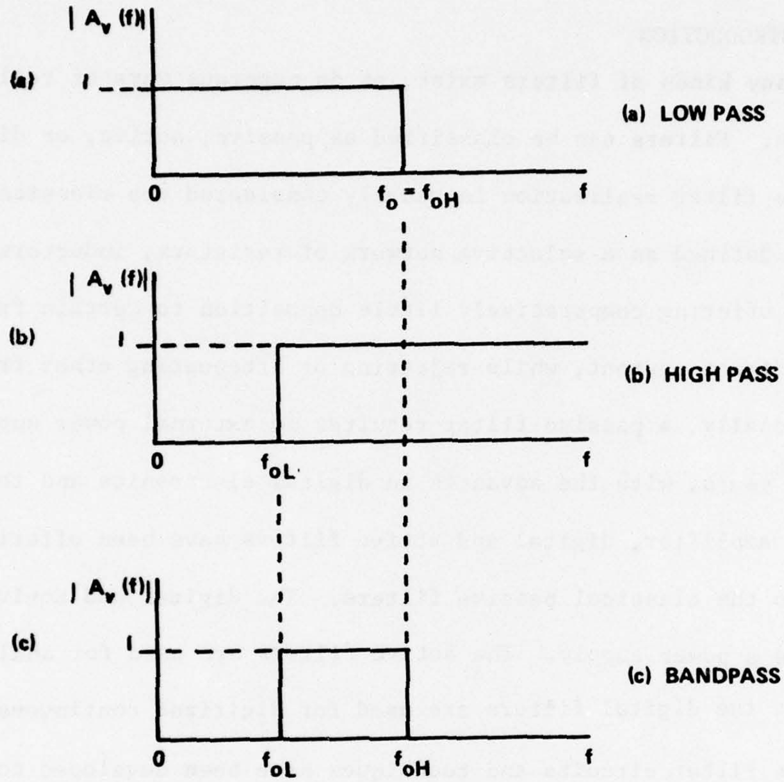

Figure 1. Ideal filter characteristics.

As shown in Figure 1a, all frequencies in the band between $0 < f < f_{oH}$ will be passed with no original signal gain change, whereas frequencies greater than f_{oH} will be completely rejected. In a like manner, for the highpass filter shown in Figure 1b, all frequencies $f < f_{oL}$ will be blocked while frequencies $f > f_{oL}$ will be passed with no gain change. Figure 1c depicts the "ideal" bandpass filter characteristics. Only those frequencies that lie in the passband $f_{oL} < f < f_{oH}$ will be processed by the device with no effect on the amplitude of the input signal.

Exhaustive attempts have been made to realize these "ideal" filter characteristics, but these filter characteristics have been unrealizable

with existing physical devices. Some of the better known methods that have attempted to duplicate the "ideal" filter characteristics are the Butterworth, Chebyshev and Cauer filters.

The Butterworth lowpass approximation yields an input/output transfer function, H(s), that is in polynomial form. This polynomial exhibits maximally flat behavior at the origin. If one is only interested in the signal loss as a function of frequency, the only virtue of the Butterworth approximation is its mathematical simplicity. A very slow transition between the passband and stopband is sacrificed for this simplicity. For a very sharp transition region, a very high order polynomial is required.[2] The Butterworth response for various values of "n" is given by the equation:[3]

$$|B_n(\omega)| = \sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^{2n}} \quad . \tag{1}$$

A plot for various values of "n" is shown in Figure 2. As "n" increases, the lowpass filter frequency response approaches but never reaches the characteristics exemplified by the ideal lowpass filter shown in Figure 1. The Butterworth filter approximation to the ideal lowpass filter is good in the low frequency region, but the approximation becomes poor in the cutoff frequency region. For n = 7, the normalized Butterworth polynomial would be:

$$(S + 1)(S^2 + 0.455S + 1)(S^2 + 1.247S + 1)(S^2 + 1.802S + 1) \quad . \tag{2}$$

A typical realization of this equation using operational amplifiers is shown in Figure 3.[4]

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[2] R.W. Daniels, Approximation Methods for Electronic Filter Design (New York: McGraw-Hill Book Company, 1974) p. 18.

[3] Millman, Integrated Electronics p. 549.

[4] Ibid. p.552.

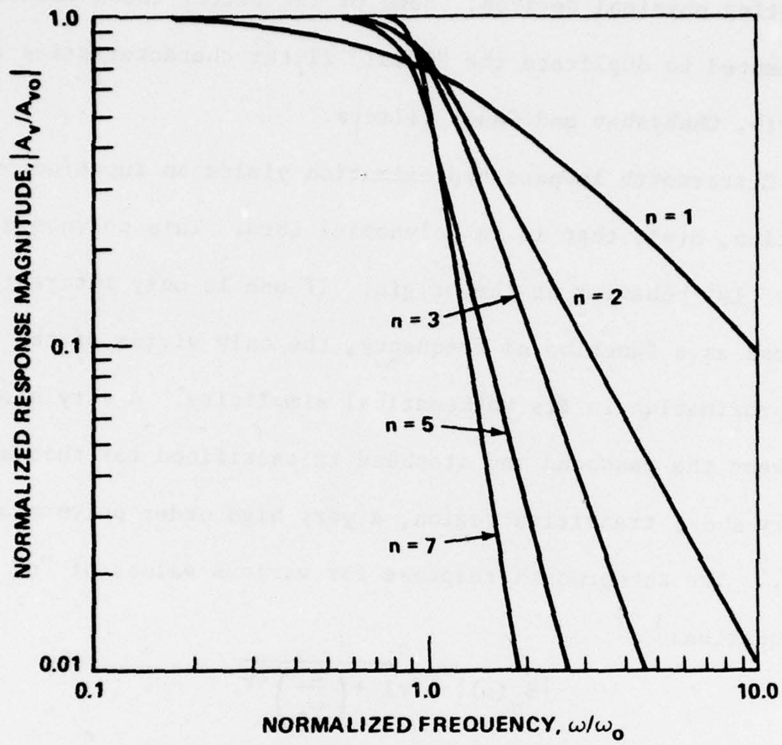

Figure 2. Butterworth lowpass filter frequency response.

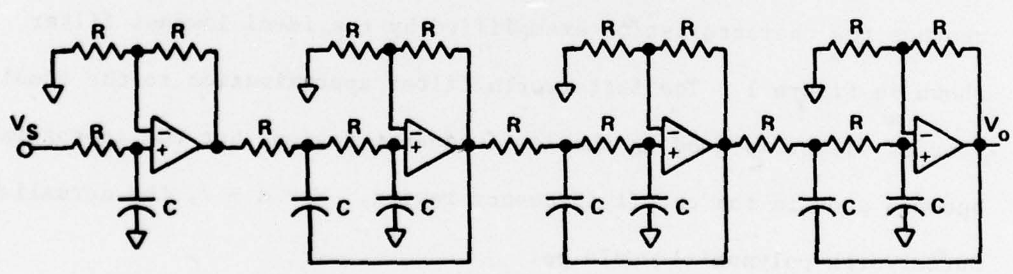

Figure 3. Butterworth filter realization for n = 7.

If a band of frequencies is of interest, a Chebyshev type of approximation is useful. This method considers the approximation error throughout the frequency interval of interest. A function h(ω) is a Chebyshev approximation of f(ω) if the available parameters are adjusted so the magnitude of the largest error is minimized. The minimized error

yields a function whose property is equiripple; i.e., the error oscillates between maximums and minimums of equal amplitude.[5] As in the Butterworth case, the Chebyshev approximation yields a polynomial for H(s). Because of the equiripple nature of the Chebyshev approximation, the transition region is much steeper than the Butterworth approximation. H(s) for the Butterworth and Chebyshev approximations is a polynomial; that is, all the attenuation poles are at infinity; therefore, a filter (passive) of degree "n" can be realized by using a total of "n" inductors and capacitors.

Filters equiripple in the passband and stopband are called Cauer filters, Zolotarev filters, or Darlington filters. These filters are found by using elliptic functions and are also referred to as elliptic filters. Elliptic filters have equal loss maximums in the passband and equal loss minimums in the stopband; thus, elliptic filters are often said to be equiripple in the passband and stopband. Elliptic filters will usually be of lower degree than Butterworth or Chebyshev type filter approximations.[6]

Each filter approximation has its strong points and its shortcomings, but all have one thing in common. As the accuracy requirements become more critical, the mathematics involved to realize a desired implementation becomes complex thus increasing reliance on computer techniques. Further, the physical realization of high order filter circuits becomes unwieldy and difficult to implement.

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[5] Daniels, Approximation Methods p. 21.

[6] J. L. Herrero and G. Willoner, Synthesis of Filters (New Jersey: Prentice-Hall, Inc., 1966) p. 64.

Statement of the Problem

The Butterworth, Chebyshev, and Cauer filter approximations have individual advantages and disadvantages attempting to approximate the "ideal" filter characteristics shown in Figure 1. The Butterworth approximation has the disadvantage of requiring a high order transfer function to realize a sharp transition region. The Chebyshev approximation adjusts parameters to minimize the magnitude of the largest error; that is, the error oscillates between maximums and minimums of equal amplitude. The Cauer or elliptic approximation is also equiripple in the passband and stopband. These approximation methods are all difficult to design where stringent accuracy is a requirement.

Realization of the ideal filter characteristics would, therefore, be desirable, but realization of these characteristics in a simple and straightforward manner without resorting to complex mathematics or computer techniques in the design phase would be equally ideal. Such a detection technique is suggested to be possible which closely approximates the cutoff points and center frequency of the ideal filter with such accuracy that no present passive or active filter can duplicate the sharpness of its cutoff points. The physical realization of this digital device can be implemented with relatively few and simple calculations in a straightforward design effort.

The proposed technique will be demonstrated in the following order:

a. Development of digital detector theory

b. General design synthesis of detection filter

c. Typical application example to illustrate the design procedure.

II. GENERAL SYNTHESIS OF A DETECTION FILTER

Classical passive filters face strong competition from digital and active filters. This is due to the fact that, as large scale integration becomes more practical and less expensive, the cost of digital filters will fall and the filters will offer even stronger competition for the passive and active filters presently used in processing of analog signals. With digital filters becoming more competitive and as more is learned about them, applications will be found that were thought impractical or impossible in earlier years.

With these thoughts in mind, consideration will be given to a technique that can very accurately detect the center frequency F_C, and high and low frequency cutoff points F_H and F_L, respectively, of a bandpass filter. This technique is equally well suited for realizing highpass and lowpass filter characteristics as for realizing the bandpass characteristics.

Consider Figures 4 through 6. Figure 4 shows a typical sinusoidal input signal F_i, and Figure 5 shows the signal after conditioning and shaping where T_x and T_y are the Schmitt triggers "on" delay time and "off" delay times, respectively, associated with one half of the input signal, $T_i/2$. From Figures 4 through 6, the following equation can be written:

$$\frac{T_i}{2} = (T_x + T_y) + T_z + nTo + eTo \quad . \qquad (3)$$

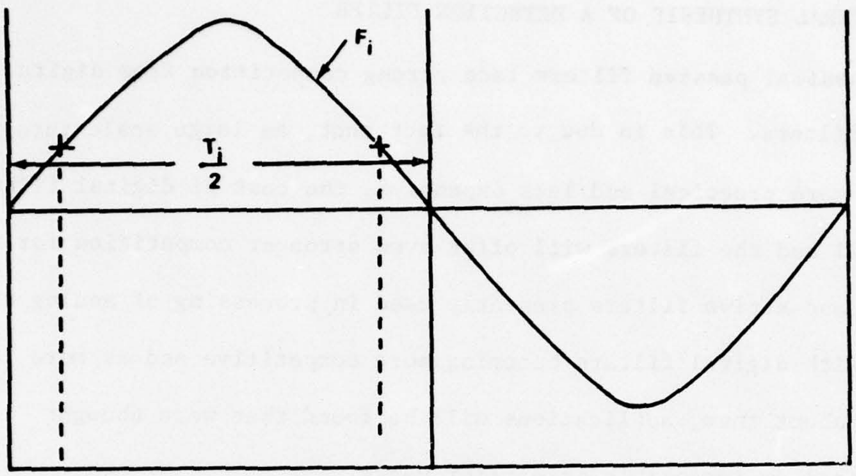


Figure 4. Input signal - sinusoidal or squarewave.

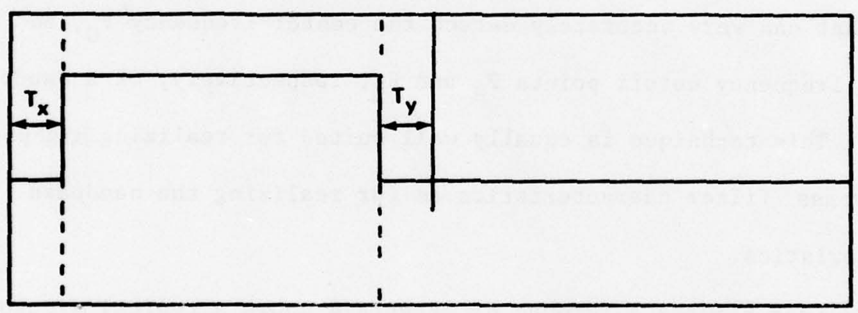


Figure 5. Schmitt shaping of input signal.

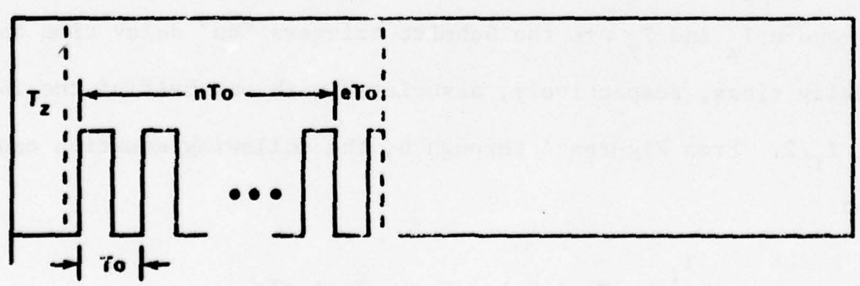


Figure 6. Counter input pulses.

Let C = n + ne be the total number of counts and let:

$$Ca = \begin{cases} C \text{ if } C \leq 2^a - 1 \\ \\ C - (H-1)(2^a) \quad \text{if } C \geq 2 \end{cases} \tag{4}$$

where "a" is the number of variables in the Karnaugh map filter and H represents the harmonics, (2, 3,...). Harmonics, as used in this paper, are multiples of a digital count. To simplify the analysis let the input signal F_i be a squarewave input; then $(T_x + T_y) \approx 0$ and T_z is small compared to $(C \cdot To)$.

From equation (3)

$$\frac{T_i}{2} \approx nTo + eTo \tag{5}$$

and

$$F_i \approx \frac{1}{T_i} \approx \frac{1}{2(nTo + eTo)} \approx \frac{F_o}{2(n+e)} \approx \frac{F_o}{2C}\ , \tag{6}$$

where

e > 0.5 Assuming 50% Duty Cycle of F_o .

Because the a bit binary counter sees only the counts C_a, then

$$F_i = \frac{F_o}{2\left[Ca + (H-1)\ 2^a\right]}\ ,$$

where H = fundamental, 2, 3, 4 ...

The bandwidth of the filter is dependent on the spread of Karnaugh map cells used in the formation of the filter design equation. A single cell in the Karnaugh map is selected to represent the center frequency F_C. Cells prior to the center frequency cell represent a high frequency deviation, +ΔF, while cells after the center frequency represent a low frequency deviation, -ΔF. This is due to the controlling gate frequency

F_i. A high frequency input signal, F_i, allows fewer pulses to be generated by the gated pulse generator F_o, while a low frequency input signal, F_i, allows more pulses to be counted. It is important to note that the filter is nonsymmetrical; that is, $+\Delta F$ does not equal $-\Delta F$.

If a four bit counter is used in counting the pulses generated by the internal oscillator, F_o, then a four variable Karnaugh map would be required to map these four variables. Now the total number of Karnaugh map cells in the filter is given by:

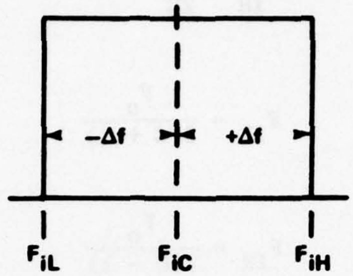
$$K = K' + 1 \tag{7}$$

where

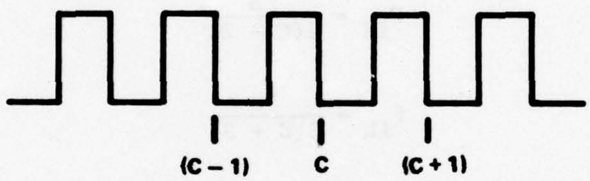
$$K' = (C_k + P) - (C_k - Q) \tag{8}$$

$$K' = P + Q \tag{9}$$

where P is the number of Karnaugh map cells above the center frequency cell C_k, and Q is the number of Karnaugh map cells below the center cell C_k. P and Q represent the high frequency cutoff and low frequency cutoff, respectively. For a symmetric filter [Figure 7(a)] $+\Delta F$ and $-\Delta F$ are equal; therefore, P is equal to Q and the number of Karnaugh map cells that would comprise the bandwidth of the filter is odd [i.e., (1, 3, 5, 7, 9 ....)]. For a count of C-1 to be detected by the counter [Figure 7(b) shows pulses being generated by the internal oscillator F_o], the gate period controlled by F_i must decrease, thereby indicating an increase in input frequency. In like manner, when the Count C+1 is detected this indicates the period of F_i has increased, thereby increasing the number of pulses counted by the counter and signaling a decrease in frequency.



a. Symmetrical Filter Characteristics



b. Oscillator Pulses F_o.

Figure 7. Characteristic waves.

Equation (6) gives

$$F_i \approx \frac{F_o}{2C} \ . \tag{10}$$

Then the cutoff points are given by the following equations:

$$F_{iH} = \frac{F_o}{2(C - \frac{K-1}{2})} \tag{11}$$

and

$$F_{iL} = \frac{F_o}{2(C + \frac{K+1}{2})} \ . \tag{12}$$

If K = 1, K' = 0, this implies that P = Q = 0; therefore, using (11) and (12), the following equations emerge:

$$F_{iH} = \frac{F_o}{2C} \tag{13}$$

and

$$F_{iL} = \frac{F_o}{2(C + 1)} . \tag{14}$$

For K = 3 (P = Q = 1)

$$F_{iH} = \frac{F_o}{2(C - 1)} \tag{15}$$

$$F_{iL} = \frac{F_o}{2(C + 2)} . \tag{16}$$

For K = 5 (P = Q = 2)

$$F_{iH} = \frac{F_o}{2(C - 2)} \tag{17}$$

$$F_{iL} = \frac{F_o}{2(C + 3)} \tag{18}$$

etc.

The bandwidth of the device is given by

$$B = F_{iH} - F_{iL} \tag{19}$$

$$B = \frac{F_o}{2(C - \frac{K-1}{2})} - \frac{F_o}{2(C + \frac{K+1}{2})} . \tag{20}$$

Simplification yields:

$$B = \frac{F_o}{2} \left[\frac{K}{C^2 + C - \frac{K^2-1}{4}} \right] . \tag{21}$$

The term in brackets in equation (21) is a dimensionless quantity that modifies $F_o/2$. Let

$$M_K^C = \frac{K}{\left(C^2 + C - \frac{K^2-1}{4}\right)} \quad . \tag{22}$$

Since K << C, then $M_K^C << 1$. By substituting values of K = 1, 3, 5... and letting C vary, a family of curves of C versus M_K^C can be generated as shown in Figure 8. For example, let K = 3 and C = 24; then

$$M_3^{24} = \frac{3}{(24^2 + 24 - \frac{9-1}{4})} \tag{23}$$

$$M_3^{24} = 5.02 \times 10^{-3} \quad . \tag{24}$$

Then equation (21) can be written as

$$B = \frac{F_o}{2} M_K^C \quad . \tag{25}$$

If C >> K, then M approaches zero as C approaches infinity and

$$M_K^C \approx \frac{K}{C(C + 1)} \quad , \tag{26}$$

and, since $C^2 >> C$, then

$$M_K^C \approx \frac{K}{C^2} \quad . \tag{27}$$

Delta Frequency Deviation

+ΔF can be defined as that frequency difference upward from the center frequency F_i, and, in a like manner, -ΔF is that frequency downward from the center frequency F_i. Using equations (10) through (12), +ΔF and -ΔF are found to be

$$+\Delta F = \left[\frac{F_o}{2\left(C - \frac{K-1}{2}\right)} - \frac{F_o}{2C}\right] \tag{28}$$

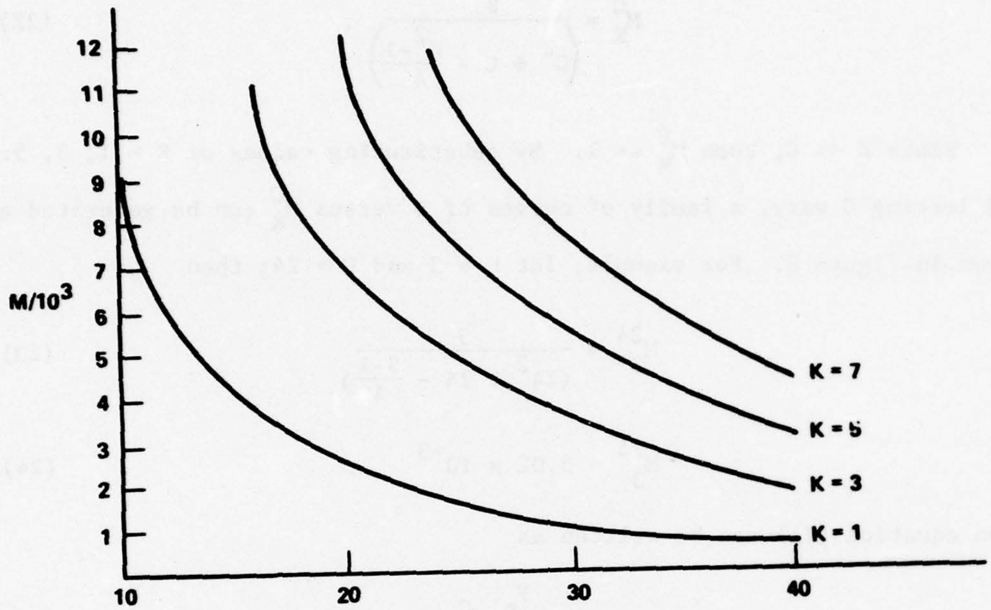


Figure 8. Bandwidth parameter M_K^C versus C.

$$+\Delta F = \frac{F_o}{2}\left[\frac{\frac{K-1}{2}}{C(C - \frac{K-1}{2})}\right] \tag{29}$$

and

$$-\Delta F = \left[\frac{F_o}{2C} - \frac{F_o}{2\left(C + \frac{K+1}{2}\right)}\right] \tag{30}$$

$$-\Delta F = \frac{F_o}{2}\left[\frac{\frac{K+1}{2}}{C(C + \frac{K+1}{2})}\right]. \tag{31}$$

For a filter to exemplify symmetrical bandpass characteristics, $+\Delta F$ must equal $-\Delta F$. To insure near symmetry, certain conditions must be met by C and K. Even P = Q does not insure $+\Delta F = -\Delta F$. Now if $+\Delta F$ equals $-\Delta F$, then the following conditions must exist:

$$\left[\frac{\frac{K-1}{2}}{C(C-\frac{K-1}{2})}\right] = \left[\frac{\frac{K+1}{2}}{C(C+\frac{K+1}{2})}\right]. \tag{32}$$

For this condition to exist

$$C = \left[\frac{K^2-1}{2}\right] \tag{33}$$

and, because C >> K, $\Delta F \neq -\Delta F$.

In many situations nonsymmetrical filter characteristics may be desired or even required, but in those cases where a symmetrical bandwidth is desired, an apparent center frequency F_i' can be reached where $+\Delta F'$ appears to equal $-\Delta F'$.

$$F_i' = \frac{F_{iH} + F_{iL}}{2} \tag{34}$$

$$F_i' = \frac{\left[\frac{F_o}{2\left(C-\frac{K-1}{2}\right)}\right] + \left[\frac{F_o}{2\left(C+\frac{K+1}{2}\right)}\right]}{2} \tag{35}$$

$$F_i' = \frac{F_o}{2C}\left[\frac{C+\frac{1}{2}}{C+1-\frac{K^2-1}{4C}}\right]. \tag{36}$$

Now, when the term

$$\left[\frac{K^2-1}{4C}\right] = \frac{1}{2}, \tag{37}$$

then the apparent frequency F_i' equals the actual frequency F_i and

$$C = \left[\frac{K^2-1}{2}\right]. \tag{38}$$

Harmonic Considerations

A harmonic as used here is defined to be a multiple of digital counts exceeding the capability of the counter. Because a four variable map is being considered, this implies a four bit counter is also being

considered. One of the operating characteristics of a four bit binary counter is that it counts zero through fifteen in a binary weighted fashion, the next count after the fifteenth count is zero, etc. For the counter to give the actual number of counts detected during this time interval, the number of counts must be between zero and fifteen. If a greater number of pulses is presented, which is invariably the case, some multiple of fifteen and a remainder will be detected by the counter.

Because the filter under consideration here depends on the number of counts detected by the binary counter, which could very well be a multiple of $(2^a + Ca)$, several passband frequencies could be detected.

The harmonics would be a function of the internal oscillator, F_o, and the input frequency, F_i. Suppose, for example, C = 24 and a = 4; then

$$C = Ca + 2^a \tag{39}$$

$$Ca = 8 \tag{40}$$

The filter would detect any frequency F_i that would place Ca in the counter or its multiples; i.e., 8, 16+8, 32+8, 48+8, ... as an acceptable signal detection.

For "a" small, which would not be the normal case,

$$F_i = \frac{F_o}{2(Y)} \quad Y = 8, 24, 40, 56 \ldots \tag{41}$$

$$F_i = \frac{F_o}{24}, \frac{F_o}{40}, \frac{F_o}{56} \ldots \tag{42}$$

$$F_i = \frac{F_o}{2(Ca + (H-1)\,2^a)} \quad H = 1,2,3,4,\ldots \tag{43}$$

To eliminate unwanted harmonics, a precounter as shown in Figure 9 could be incorporated into the circuit to divide evenly the count specified by $(H-1)2^a$. The count Ca would be detected as the remainder of C.

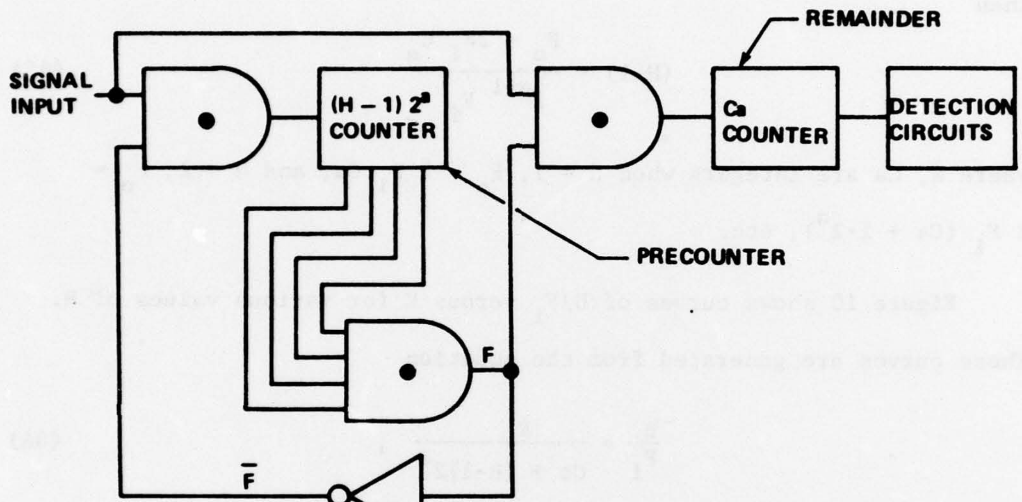


Figure 9. Harmonic elimination using a precounter.

The circuit shown in Figure 9 would function as follows. The first $(H-1)2^a$ counts would be accepted by the precounter. When this counter reached its maximum count (i.e., 111...1),the output of the AND gate, F, would lock out any further input pulses, and the remaining input pulses would be applied to Ca counter and detected as the remainder or overflow of the precounter. With this circuit all unwanted harmonics would be eliminated.

Because the bandwidth and center frequency are functions of the counter harmonics, a development of F_o, F_i, and B relative to the harmonics H is desirable.

Because

$$F_i = \frac{F_o}{2(Ca + (H-1)2^a)} , \tag{44}$$

then

$$(H-1) = \frac{F_o - 2F_i C_a}{2^{a+1} F_i} \tag{45}$$

where H, Ca are integers when H = 1, $F_o = 2 F_i$ Ca, and H = 2, $F_o = 2 F_i (Ca + 1 \cdot 2^a)$, etc.

Figure 10 shows curves of B/F_i versus K for various values of H. These curves are generated from the equation

$$\frac{B}{F_i} = \frac{K}{Ca + (H-1)2^a} , \tag{46}$$

and will prove helpful in various calculations.

Considering the circuit operation in a more general manner, Figure 11 shows a block diagram of the detector system. The circuit can be divided into four basic divisions:

1. Signal conditioning
2. Gating
3. Timing
4. Decoding.

The signal conditioning is comprised of the threshold detector. Gating is comprised of the gated oscillator, NAND gate, counter, and latch. The monostable multivibrator controls the timing events, and decoding logic constitutes the decoding.

The input signal, F_i, is applied to the threshold detector. Here the signal is threshold detected and conditioned so the output signal is

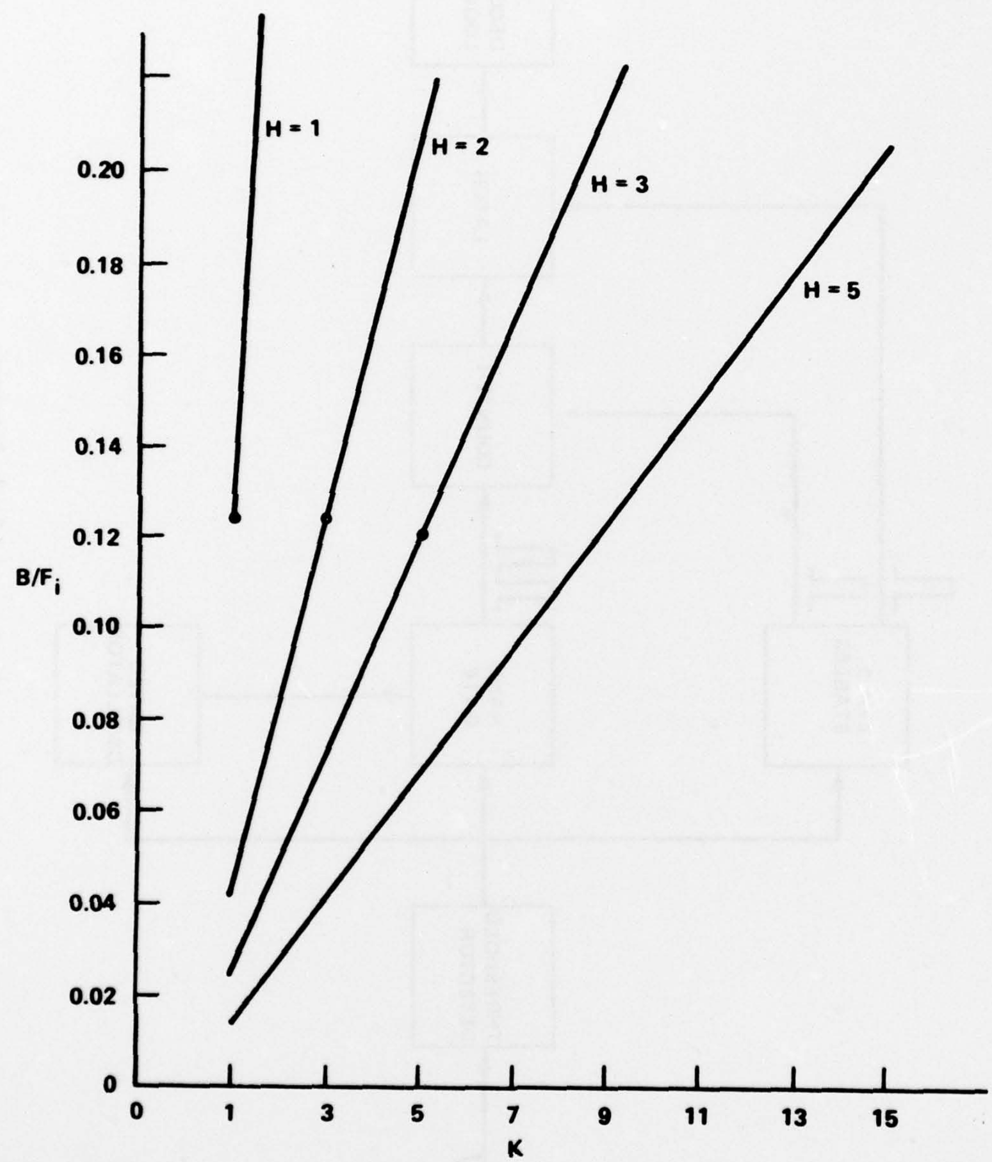


Figure 10. B/F_i versus K for H = 1, 2, 3, 5.

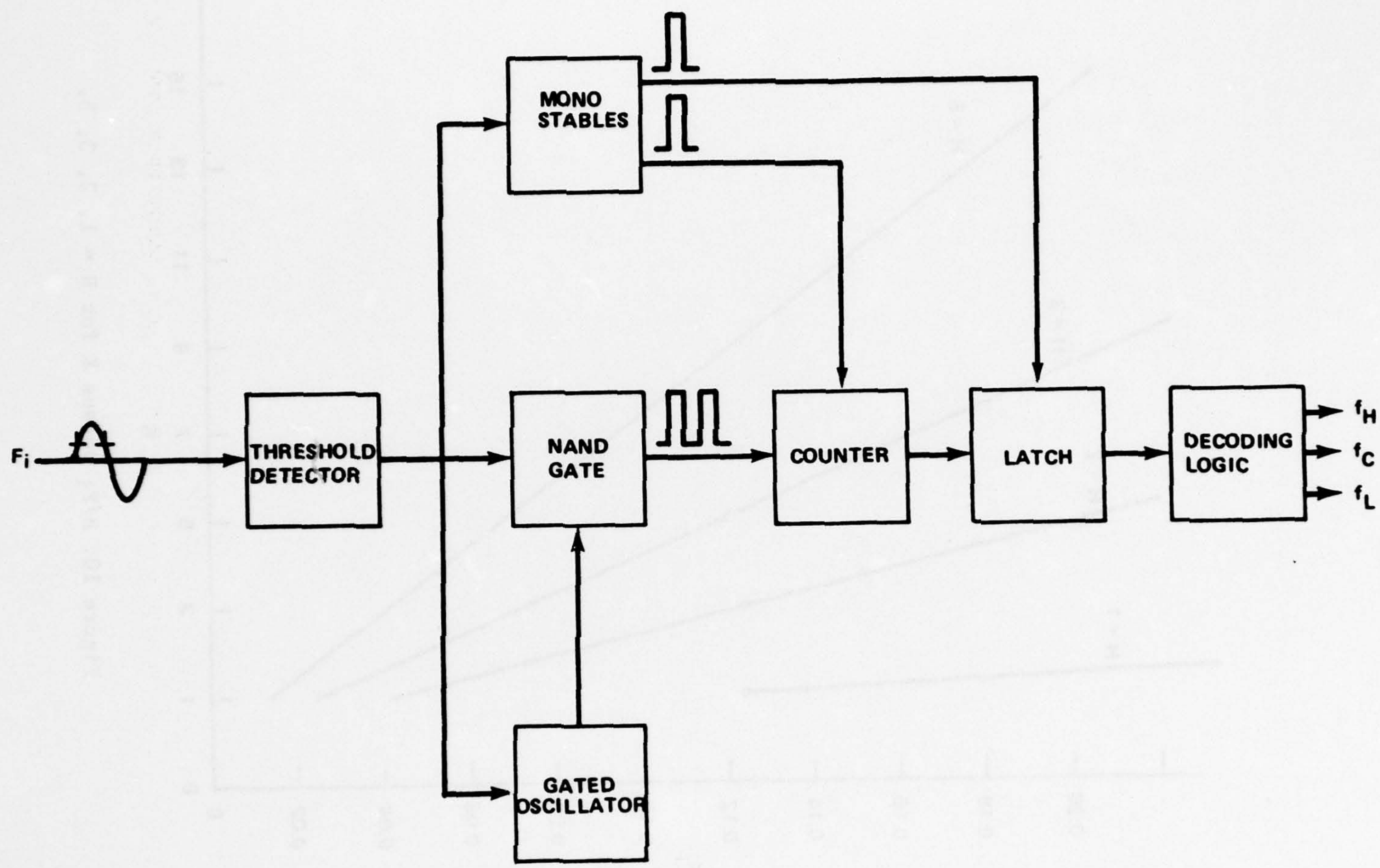


Figure 11. System block diagram.

a squarewave with a period comparable to the sinusoidal input signal. Only the positive portion of the input signal is detected. During the time the input signal is in its negative portion, various circuit activities are carried on that will be discussed later. Also, the input signal is conditioned so the squarewave output is compatible with standard logic levels. From the threshold detector, the conditioned input signal is applied to the timing and gating circuitry. For discussion purposes suppose that F_i is "positive going." This enables the gating circuitry by applying a positive voltage to one half of a NAND gate and exciting the gated oscillator. The output from the gated oscillator is then applied to the second input of the NAND gate. The output from the NAND gate is then a series of pulses that is a direct function of the period of the input signal, F_i.

The frequency of the gated oscillator is determined so, for a given input period, T_i, only a predetermined number of pulses can be generated by the NAND gate. These pulses represent a pulse count on a binary weighted n-variable Karnaugh map. This Karnaugh map cell is indicative of the center frequency of the input signal, F_i. If the frequency of the input signal should increase, the period will decrease and fewer pulses will be allowed through the NAND gate. Decoding procedures establish the cell on the Karnaugh map that represents the upper cutoff frequency F_H, thus establishing the upper cutoff frequency F_H. In a similar manner, should the frequency of the input signal decrease, the period will increase allowing more pulses to be gated through the NAND gate. This increase in pulses establishes another cell on the Karnaugh map representing the lower cutoff frequency F_L.

With the detection frequencies F_L, F_C, and F_H established and represented on the Karnaugh map, the pulses gated through the NAND gate are applied to a four bit binary counter. The counter counts the pulses generated by the gated oscillator as a function of the period of the incoming signal F_i. Because the counter is a four bit device, this implies that a four variable Karnaugh map is used to designate the various frequency cells. This data is then presented to a latch which holds the data, then in turn gates the data to the decoding logic.

The decoding logic is derived directly from the Karnaugh map, the cells of which represent the F_L, F_C, and F_H. Using standard Karnaugh mapping techniques, the hardware realization for a given function can then be implemented using standard two level transistor-transistor logic (TTL) as shown in Figure 12.

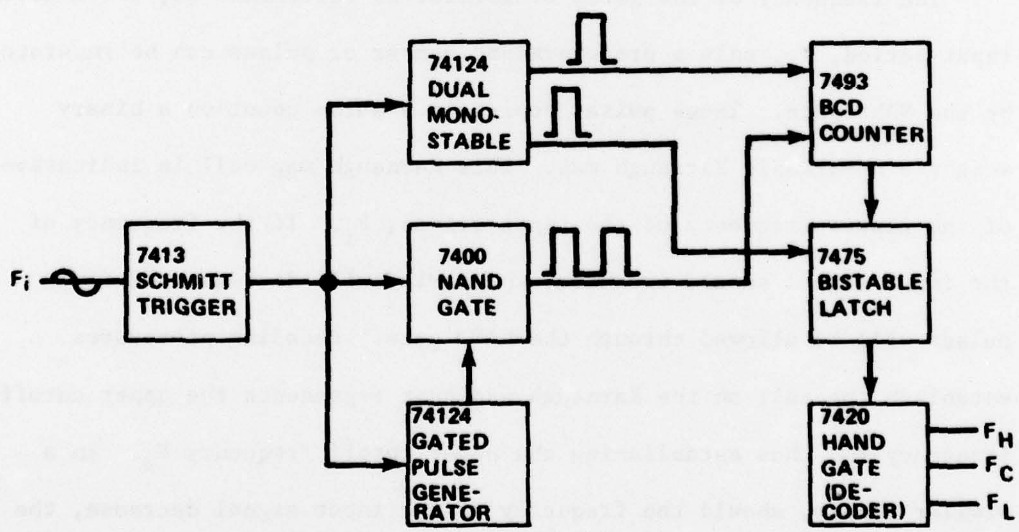


Figure 12. System implementation using standard TTL logic.

Frequency verification occurs during the time the input signal, F_i, is a positive level signal. When the input signal is a negative level signal the monostable multivibrators perform the timing or "housekeeping" tasks. As the input signal begins its transition from a positive to a negative level signal, the NAND gate and the gated oscillator are inhibited and the monostable multivibrators are enabled. The first monostable generates a pulse that latches the data from the counter to the decoding logic for proper frequency verification. At the completion of this latching pulse a second monostable multivibrator is initiated and a pulse is generated that resets the four bit binary counter to zero. After the completion of these events the system is ready to repeat the cycle of counting pulses as a result of the input signals period, latching, verifying and reseting.

III. TYPICAL APPLICATION EXAMPLE

This chapter is concerned with the detail design of a filter for a typical application. A logical question is, "What accuracies can be expected from this device?" It should be noted that amplitude modulated information is not available at the outputs of this device. The outputs provide extremely accurate and sharp cutoff points for the upper and lower frequencies of the desired bandwidth as selected by the designer. The bandwidth output from this device approaches the ideal filter bandwidth. The ideal filter assumes vertical cutoff lines ("skirts") at the bandpass end points. This filter detects these end points precisely and provides the ideal vertical cutoff lines except for the propagation delay time associated with the physical device used in the decoding logic which is typically 25 nsec.

To demonstrate a typical example, suppose design of a filter is desired that will have a center frequency F_c of 400 Hz. Let C, the total number of counts as a function of F_o, be 23 and assume a three cell Karnaugh mapping which implies K = 3. From this information can be determined the bandwidth B, the frequency deviation $+\Delta F$ and $-\Delta F$, and the internal oscillator frequency, F_o.

The determination of F_o can be obtained using equation (10) which is

$$F_i \approx \frac{F_o}{2C} \tag{47}$$

and

$$F_o = 2C\ F_i \tag{48}$$

$$F_o = 2CF_i = 2(23)(400) \tag{49}$$

$$F_o = 18.4 \text{ KHz} \quad . \tag{50}$$

The bandwidth is evaluated by using equation (25) and Figure 8 where (25) is

$$B = \frac{F_o}{2} M_K^C \quad . \tag{51}$$

Using Figure 8 yields a value for M_k^C of

$$M_3^{23} = 5.45\ (10^{-3}) \quad . \tag{52}$$

Then, the bandwidth becomes

$$B = M_3^{23} \frac{F_o}{2} = \left[5.45\ (10^{-3})\right] X \left[\frac{18.4\ (10^3)}{2}\right] = 50.14 \text{ Hz} \tag{53}$$

$$B = 50.14 \text{ Hz} \quad . \tag{54}$$

The frequency deviations can be determined from equations (29) and (31).

$$+\Delta F = \frac{F_o}{2}\left[\frac{\frac{K-1}{2}}{C\left(C - \frac{K-1}{2}\right)}\right] = \frac{18.4(10^3)}{2}\left[\frac{1}{23(23-1)}\right] \text{Hz} \tag{55}$$

$$+\Delta F = 18.2 \text{ Hz} \tag{56}$$

$$F_H = 400 + 18.2 = 418.2 \text{ Hz} \tag{57}$$

$$-\Delta F = \frac{F_o}{2}\left[\frac{\frac{K+1}{2}}{C\left(C + \frac{K+1}{2}\right)}\right] = \frac{18.4(10^3)}{2}\left[\frac{2}{23(23+2)}\right] \text{Hz} \tag{58}$$

$$-\Delta F = 32 \text{ Hz} \tag{59}$$

$$F_L = 400 - 32 = 368 \text{ Hz} \quad . \tag{60}$$

The filter bandwidth can readily be observed to be nonsymmetrical. To obtain a symmetrical bandwidth use is made of equation (36) which gives the apparent frequency F_i':

$$F_i' = \frac{F_o}{2C}\left[\frac{C + \frac{1}{2}}{C + 1 - \frac{K^2-1}{4C}}\right] Hz \qquad (61)$$

$$F_i' = \frac{18.4(10^3)}{2 \times 23}\left[\frac{23 + \frac{1}{2}}{23 + 1 - \frac{8}{92}}\right] = (400)\ (0.983)\ Hz \qquad (62)$$

$$F_i' = 393\ Hz \qquad (63)$$

$$+\Delta F' = (F_H - F) = 418\text{-}393\ Hz \qquad (64)$$

$$+\Delta F' = 25\ Hz \qquad (65)$$

$$-\Delta F' = (F' - F_i) = 393 - 368\ Hz \qquad (66)$$

$$-\Delta F' = 25\ Hz\ . \qquad (67)$$

IV. CONCLUSIONS AND RECOMMENDATIONS

Using Karnaugh mapping methods has shown that a filter detection scheme can be implemented for an incoming signal F_i that approaches the ideal filter characteristics of a bandpass filter. The same ease and simplicity shown for the bandpass filter implementation is also applicable for realizing near ideal lowpass or highpass filter characteristics.

This detection method has also been shown to realize an arbitrary center frequency and the upper and lower cutoff frequencies in an extremely precise and accurate manner rather than the usual -3 dB specification at some desired frequency as in the case of the Butterworth filter. The realization of the upper and lower cutoff frequencies with the digital filter shaping characteristics approximates $n = \infty$ using the Butterworth parameters. In terms of these described digital techniques, the cutoff frequencies can be detected in approximately 25 nsec.

As with most research investigations there are unsolved problems or areas where further research is desired. Other areas which should be investigated are:

1. High frequency detection - The upper frequency is presently limited by the internal oscillator. The existing design has an upper frequency limit of 15 MHz. If the assumption is made that the internal oscillator, F_o, should be 10 times as fast as the incoming signal F_i, this places an operational frequency restriction on the complete system of 1.5 MHz. Therefore, this area could be explored to determine if the frequency of operation could be extended into a higher frequency range.

2. Multifrequency Detection Using a Microprocessor - Another consideration would be the implementation of a bipolar microprocessor. Such a device could be used to perform the Karnaugh map decoding under program control for simultaneous frequency inputs thus making the system a versatile scheme for decoding or encoding information.

3. Read Only Memory, (ROM), Decoder - Finally for consideration is the utilization of an ROM in the decoding stage. The outputs from the detection system would generate address locations to the ROM and the outputs of the ROM could then be used to configure either a closed loop or open loop control system responding to the deviations sensed by the detection system.

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